Licensing and Technology Transfer Opportunity: Manipal University

Title of Technology Available:

A Low Power-Delay Product Multiplier Unit

Brief Description of Invention:

Modified Booth Multiplier with Carry pre-computation

An 8 bit Binary Modified Booth based multiplier with carry pre-computation has been proposed with A and B as inputs and P as the final 16-bit product. The modified booth encoding is the first block of the multiplier to which the 8 bit multiplicand and multiplier are given as inputs. The second stage in the block diagram is the carry generation circuit. Here, we have integrated pre-computation logic along with the modified booth multiplication technique. The carry equations are generated separately for each column of partial products and the inputs for these equations are taken from the previous column. Carry pre-computation logic calculates all the carries for next stage in parallel, so that the computation time can be reduced. The third stage in the block diagram involves the use of XOR logic for the partial products and carry generated in each column. The output of this stage gives the final 16 bit product which is obtained in a parallel mechanism instead of sequential mechanism.

Modified Booth Multiplier with Carry pre-computation and Dynamic Range Detection

First stage of proposed architecture performs dynamic range detection which does following operations.

1. Checks if A is smaller than B or B is smaller than A. Smaller number will be considered to generate partial products.
2. Checks how many 2's complement partial product will be generated, if number of 2's partial products are more than 2, then 2's complement is performed on the input to reduction number of 2's complement partial product which in turn can reduce the power of the architecture.

The modified booth encoder generates partial products from the input which comes from Dynamic Range Detection unit. All partial products are generated at the same time. Carry pre-computation logic along with the modified booth multiplication technique has been integrated to generate all the intermediate carries. XOR logic block performs xor operation between partial products and carry generated in each column. The output of this stage gives the 16 bit product which is obtained in a parallel mechanism instead of sequential mechanism. 2's complement value of XOR logic output or normal value of XOR logic output is selected based on the select signal from Dynamic Range Detection unit.

Brief Background of Invention:

Various algorithms have been proposed for the hardware implementation of multipliers. Add and Shift is the common algorithm used in designing of multiplier. In parallel multipliers, the important parameter which is used to determine its performance is the number of partial

products which are needed to be added. Modified Booth algorithm will reduce the number of partial products during the multiplication which in turn increase the performance of the multiplier. Wallace tree based algorithm which reduces number of adding stages, can be used to improve the speed of multiplication. The efficient multiplier architecture can be designed by combining both Modified Booth algorithm and Wallace Tree algorithm. However, increasing parallelism will increase the number of shifts between intermediate sum and partial products, which may result in reducing the speed, increase the power consumption, and also increase in area because of irregular structure. On the other hand, low power and compact multiplier architectures can be implemented using serial multiplication algorithms. Serial multipliers have better performance for power consumption and area with the delay tradeoff. Depending upon the application, either parallel or serial multiplier can be selected to perform the operation. We provide a brief description of some of the studies based on different types of multiplication algorithms.

Describe the final product:

The proposed invention performs the multiplication operation at high speed and consumes less power.

Technological Domain (Keywords):

Binary Multiplier, Pre Computation (Pre Calculation or Pre Estimation), Modified Booths, High speed, Low Power, Power Delay Product, Dynamic Range Detection (Determining the range of given value on-the-go)

Proof of Concept:

NA

Stage of Development:

Advanced Prototype

Provide Information on Competitors who manufacture and/or sell similar products: NA

What are the unique advantages your innovation has compared to the competition:

Low power consumption: Dynamic Range Detection unit chooses smaller number to generate partial products and reduces number of 2's complement operation, hence reduce power consumption. As only one optimized encoder is used in unlike conventional modified booth multiplier which uses multiple booth encoders and decoders, the power consumption is also reduced.

High speed circuit: As Carry Pre-Computation unit computes all the carries in parallel using carry look ahead logic and remove dependencies between columns, the total time required to generate the product will be reduced.

A few potential companies who might be interested in this technology: Nvidia, Intel, Qualcomm, Synopsys

Intellectual Property Status: **Application#: 201841002183** and **Date of Filing: January 18, 2018**